

1 system for identifying the occurrence of a processor unit
2 reset, the system comprising:

3 timing trace apparatus responsive to signals from the
4 processor unit, the timing trace apparatus generating a
5 timing trace stream;

6 program counter trace apparatus responsive to signals
7 from the processing unit, the program counter trace
8 apparatus generating a program counter trace stream; and

9 synchronization apparatus applying periodic signals to
10 the timing trace apparatus and to the program counter trace
11 apparatus, ~~the periodic signals~~;

12 wherein the program counter trace apparatus is
13 responsive to a reset signal, the program counter trace
14 apparatus generating a reset marker signal group
15 identifying the occurrence of reset signal and relating the
16 reset signal to the timing trace stream and the program
17 execution the program counter trace stream.

18

19 Please amend Claim 2 as follows.

20

21 2. (**Currently Amended**) Original) The system as
22 recited in claim 1 wherein the reset marker signal group
23 includes a program counter address, a timing index and a
24 periodic sync ID.

25

26 3. (**Original**) The system as recited in claim 1
27 further comprising:

28 data trace apparatus responsive to signals from the
29 processing unit, the data trace apparatus generating a data
30 trace stream, wherein the periodic sync ID signals are

1 applied to the data trace apparatus provide periodic sync
2 markers in the data trace stream; and

3 wherein the host processing unit is responsive to the
4 timing trace stream, the program counter trace stream and
5 the data trace stream, the host processing unit
6 reconstructing the processing activity of the processing
7 unit from the trace streams.

8

9 4. **(Original)** The system as recited in claim 1
10 wherein the program counter trace apparatus is responsive
11 to the removal of the reset signal, the program counter
12 trace apparatus generating a reset-off marker signal group,
13 the reset-off marker signal group relating the occurrence
14 of the reset signal to the timing trace stream and the
15 program execution.

16

17 **Please amend Claim 5 as follows.**

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19 5. **(Currently Amended)** The method for
20 communicating an occurrence of a reset signal from a target
21 processor unit to a host processing unit, the method
22 comprising:

23 generating a timing trace stream, a program counter
24 trace stream, and data trace stream, and

25 in the program counter trace stream, including a
26 marker signal group indicating an occurrence of reset
27 signal and relating the occurrence to the data trace
28 stream, to the timing trace stream, and to the program
29 execution program counter trace stream.

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1 6. (**Original**) The method as recited in claim 5
2 further including:

3 in the marker signal group, including a periodic sync
4 ID, a timing index and a program counter address.

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6 7. (**Original**) The method as recited in claim 5
7 further comprising, when the reset signal is removed,
8 including in the program counter trace stream a marker
9 signal group indicating the occurrence of the removal of
10 the signal group and relating the marker signal group to
11 the timing trace stream and program execution.

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13 **Please cancel claim 8.**

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15 8. (**Cancelled**) ~~In a processing unit test~~
16 ~~environment wherein a target processor transmits a~~
17 ~~plurality of trace streams to a host processing unit, a~~
18 ~~marker signal group included in a trace signal stream, the~~
19 ~~marker signal group comprising:~~

20 ~~indicia of the occurrence of a reset signal;~~
21 ~~indicia of the relationship of the occurrence of the~~
22 ~~reset signal to the target processor clock; and~~
23 ~~indicia of the relationship of the occurrence of the~~
24 ~~reset signal to the target processor program execution.~~

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26 **Please cancel claim 9.**

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28 9. (**Cancelled**) ~~In a processing unit test~~
29 ~~environment wherein a target processor transmits a~~
30 ~~plurality of trace streams to a host processing unit, a~~

1 marker signal group included in a trace signal stream, the
2 marker signal group comprising:
3 indicia of the removal of a reset signal;
4 indicia of the relationship of the removal of the
5 reset signal to the target processor clock; and
6 indicia of the relationship of the removal the reset
7 signal to the target processor program execution.

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9 Please amend Claim 10 as follows.

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11 10. (Currently Amended) In a target processing unit
12 generating trace test signals for transfer to a host
13 processing unit, a program counter trace generation
14 apparatus comprising:
15 a storage unit;
16 a decoder unit responsive to a rest signal for storing
17 a signal group identifying the reset signal in the storage
18 unit in a first location in the storage unit, the decoder
19 unit generating a control signal;
20 a gate unit responsive to the control signal, the gate
21 unit transmitting processor signals applied thereto to the
22 storage unit for storage at defined locations, the signals
23 stored in the storage unit forming a reset sync marker; and
24 a FIFO unit coupled to the storage unit, the FIFO unit
25 receiving the reset sync marker when the reset signal
26 marker is complete, the FIFO unit transferring the reset
27 sync marker to the host processing unit.

28

29 11. (Original) The program counter trace
30 apparatus as recited in claim 10 wherein the signals

1 applied to the gate unit include a program counter address,
2 a periodic sync ID, and a timing index.

3

4 12. **(Original)** The program counter trace
5 apparatus as recited in claim 11 wherein when the reset
6 signal is removed, a reset-off sync marker is generated in
7 the storage unit.

8

9 13. **(Original)** The program counter trace
10 apparatus as recited in claim 10 wherein the reset sync
11 marker signal includes a plurality of packets.

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13 14. **(Original)** The program counter trace
14 apparatus as recited in claim 10 wherein the sync markers
15 in the FIFO unit are transferred from the unit in response
16 to control signals.

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